TECHNISCHE UNIVERSITÄT DRESDEN

Faculty of Electrical and Computer Engineering

Institute of Electromechanical and Electronic Design

A Globally-optimized Co-design Approach for Heterogeneous Systems Using Convex Optimization

Tilman Horst, Robert Fischbach, Jens Lienig
Dresden University of Technology, Dresden, Germany
www.ifte.de

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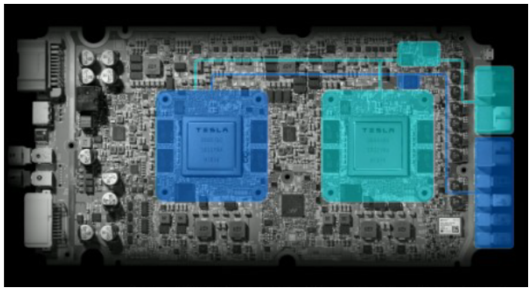
Summary

Motivation

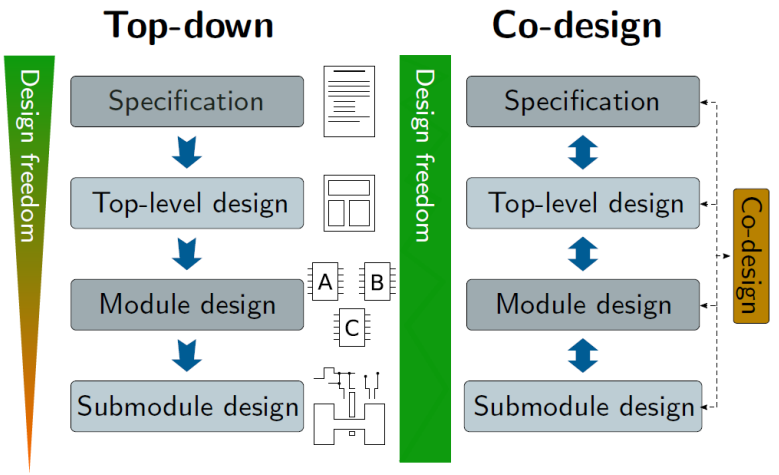
- Hardware diversity is increasing
- Dedicated circuits for AI & GPU enable orders of magnitude higher efficiency compared to general-purpose central processing units
- New integration technologies allow for high-density integration of multiple dies
- Systems are getting more complex and heterogeneous
  (e.g., Tesla full-self driving chip)
- Conventional top-down design approaches do not incorporate heterogeneity sufficiently (restricted to local, same-hierarchy optimization only)

➢ "Co-design methodology" is needed that enables optimization across hierarchy levels
(" having neighboring design levels in mind")



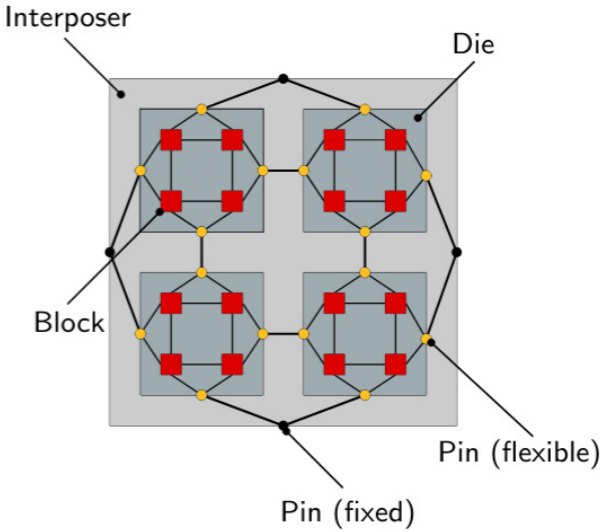
Our Approach: Co-design Methodology

- Top-down approaches are simple and straightforward, but neglect design potentials
- Proposed co-design methodology enables optimization across hierarchy levels
- Convex optimization techniques to allow for cross-hierarchical design optimization
- Holistic design approaches enable the design of more efficient hardware



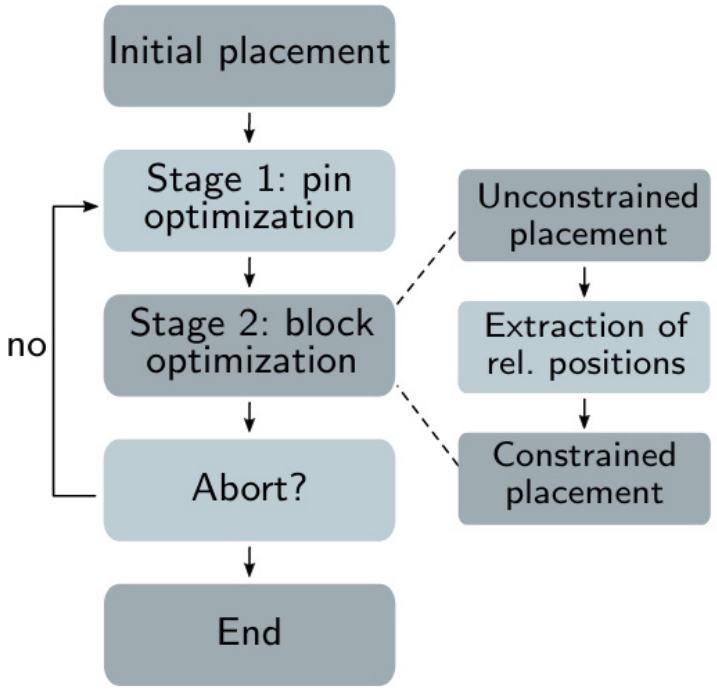
Design Example

- Hierarchical design example to illustrate our co-design methodology
- Co-design approach globally optimizes the positions of dies, blocks and related pins "across" design levels (i.e., block, die, interposer)
- Wire length is used as a measure for the quality of a design



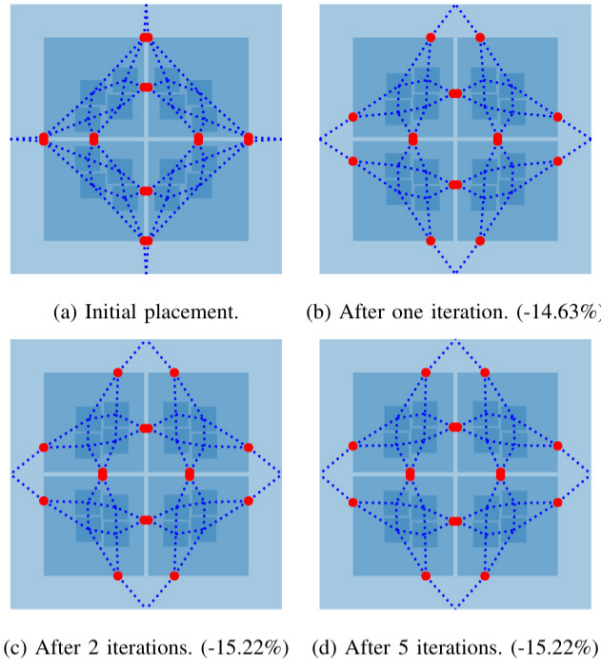
Iterative Co-design Approach

- Iterative approach to optimize the placement at each hierarchical level
- At each level, "neighboring" design levels are considered
- The ultimate goal is to find positions for all dies, blocks and pins that globally optimize the wire length



Optimization Progress

- Optimization progress after one, two and five iterations
- Minimization of top level wire length in the initial placement
- However, due to cross-hierarchical dependencies, minimizing the top level wire length only does not result in a globally optimal solution
- Our final solution slightly increases the top level wire length, but overall wire length (i.e., across all hierarchy levels) is minimized
- Algorithm converges quickly towards the global optimum

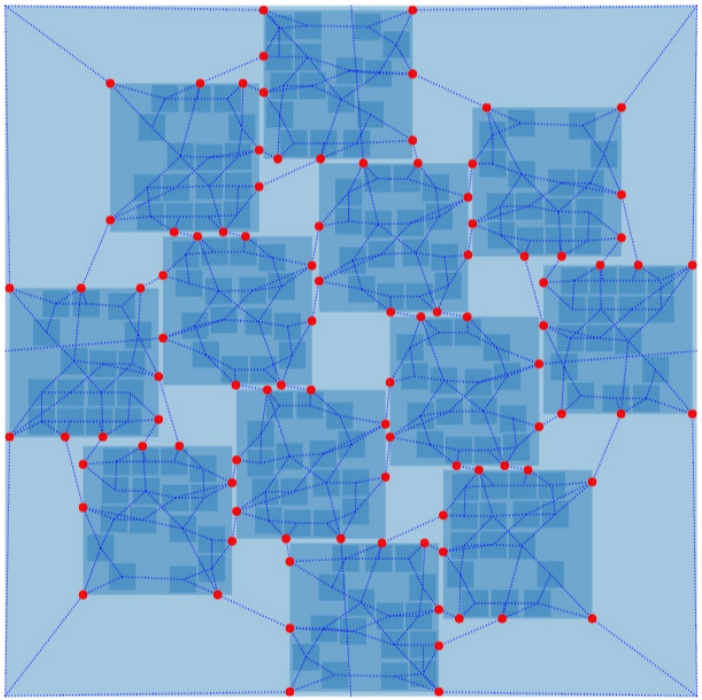


(a) Initial placement. (b) After one iteration. (-14.63%)

(c) After 2 iterations. (-15.22%) (d) After 5 iterations. (-15.22%)

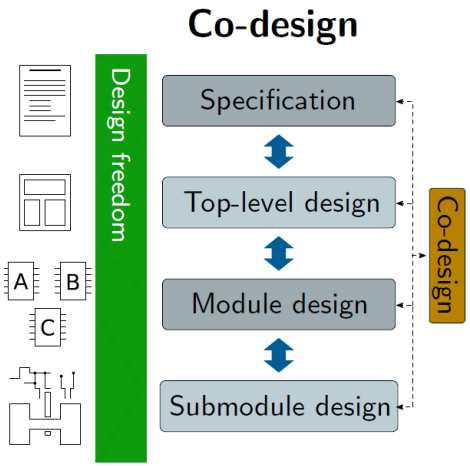
Complex Example

- As shown, more complex examples can also be solved using our algorithm
- Runtime: about 10 secs on a Intel(R) Xeon(R) CPU @ 3.00GHz



12 dies and 16 circuits blocks on each die. The resulting optimization problem consists of 492 optimization variables and about 500 constraints.

Summary



- Co-design approach enabling cross-hierarchical optimizations of complex systems
- Our contribution: Illustration of the concept via a simple example
- More complex problems can also be solved

- Details of our optimization models are outlined in the paper
- Questions: tilman.horst@posteo.de, robert.fischbach@tu-dresden.de