On the Performance Improvement of OTA in Sub-Threshold Region with Dual Supply

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Introduction

- OTA designed with CMOS technology in sub-threshold region is preferred to design low power circuits [4].
- MOSFET consumes low power in sub-threshold region and acts as BJT (Bipolar Junction Transistor).
- Although MOSFET behaves like BJT in the sub-threshold region, the drain current is still depended [5] to the $(v_{GS}-v_{th})$ as given in (1).

$$I_D = C_{OX}.\mu_{eff}\frac{W}{L}.n.V_T^2.e^{(v_{GS}-v_{th})/nV_T}[1-e^{-v_{DS}/v_T}] \qquad (1)$$

Introduction

- DTMOS technique decreases v_{th} to increase $(v_{GS}-v_{th})$.
- In this work, in addition to the DTMOS technique, v_{GS} of input transistors is increased to boost $(v_{GS}-v_{th})$ with a higher supply voltage than other transistors in the circuit [10].

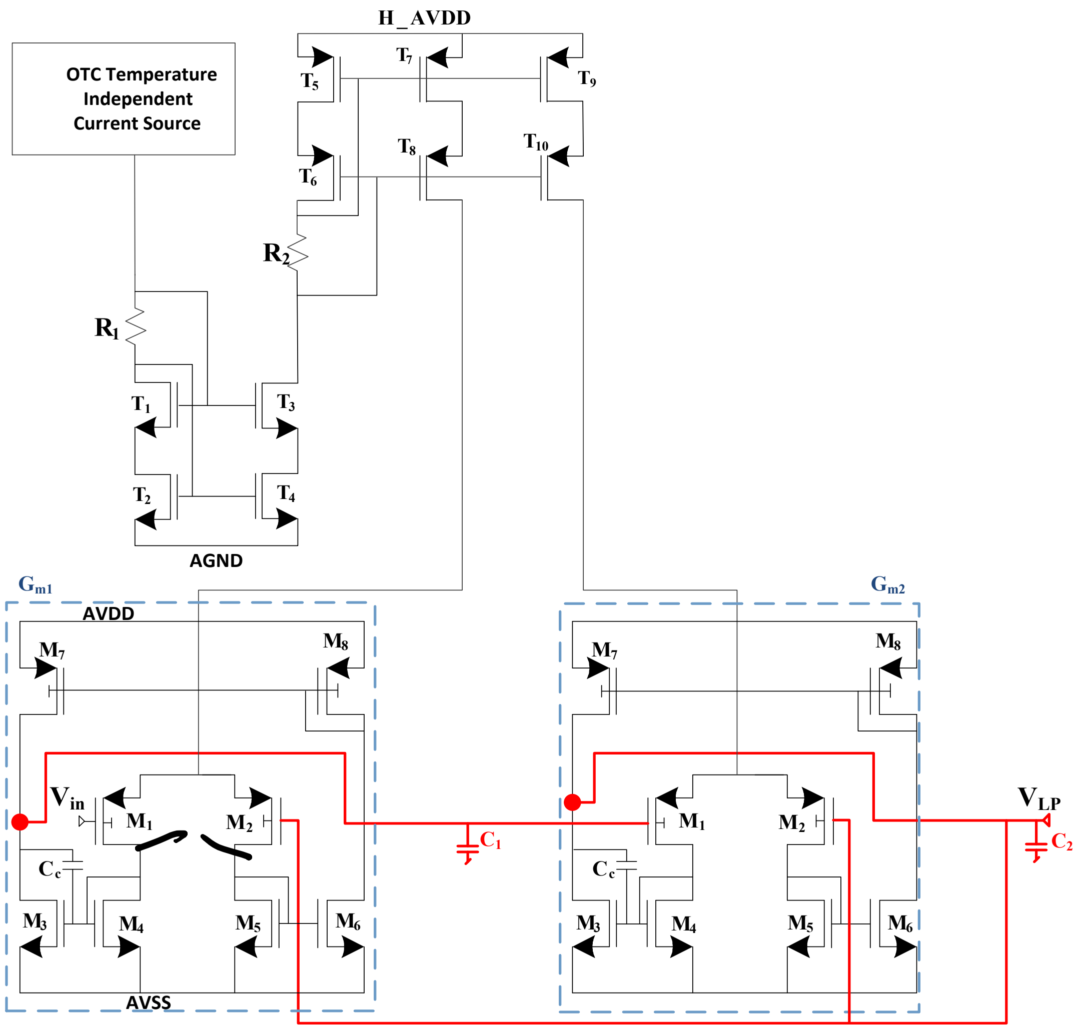

Fig. 1 *Second order low-pass filter designed in sub-threshold region with DTMOS technique, CMOS implementation*

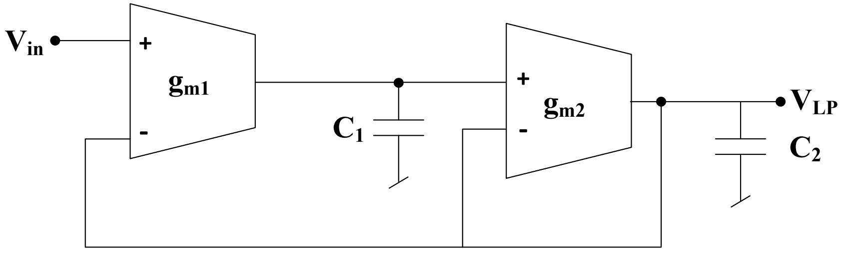

Fig. 2 *Second order low-pass filter designed in sub-threshold region with DTMOS technique, block representation of OTA-C low pass filter*

THE DESCRIPTION OF THE APPLIED CASES

Cases	AV_{DD}	AV_{SS}	H_AV_{DD}	I_B	v_{in}
(1)	150mV	-150mV	300mV	10nA	150mV$_{p-p}$ 10kHz
(2)	150mV	-150mV	400mV	10nA	150mV$_{p-p}$ 10kHz
(3)	200mV	-200mV	400mV	30nA	175mV$_{p-p}$ 10kHz
(4)	200mV	-200mV	600mV	30nA	175mV$_{p-p}$ 10kHz

$$\frac{I_o}{V_{in}} = \frac{g_{m1,2}}{g_{m4,5}}(g_{m3,7})$$	(3)
$$g_m = \frac{\partial I_D}{\partial v_{GS}} = \frac{I_D}{nV_T}$$	(4)

$$CMRR = \frac{i_D}{i_{CM}} \cong 2g_m r_l$$	**(5)**

Performance comparison of the proposed method

Cases	THD	Power	Noise	f_{-3dB}	G_m
(1)	%13.2	$20.02nW$	$1.12\mu V/\sqrt{Hz}$	331kHz	74.8nS
(2)	%2.46	$34.52nW$	$898nV/\sqrt{Hz}$	654kHz	145.3nS
(3)	%0.98	$98.4nW$	$755nV/\sqrt{Hz}$	1.85MHz	411.5nS
(4)	%0.41	$106.2nW$	$735nV/\sqrt{Hz}$	2.02MHz	449.6nS

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