Design of a 1.5 GHz Low Jitter DCO Ring in 28 nm Process

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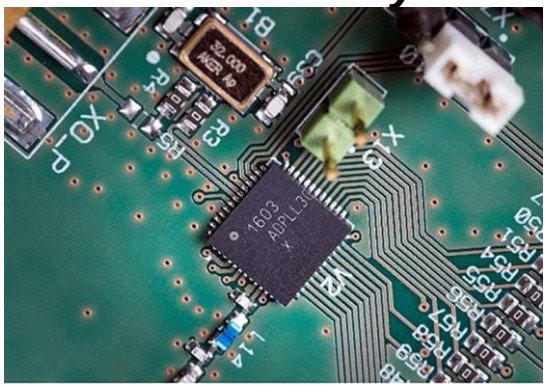
Content

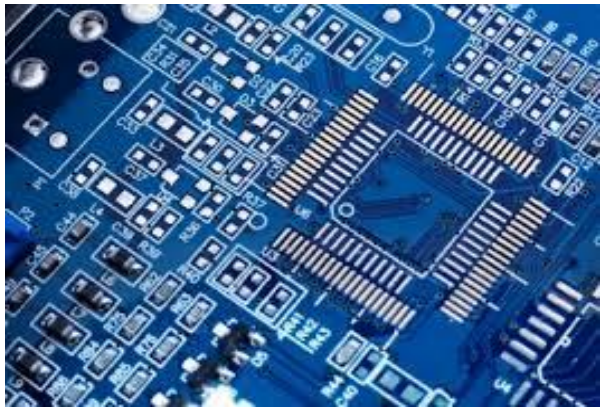
- **Context and introduction**
- DCO architecture and design
- Results and conclusion

Motivation for ADPLL

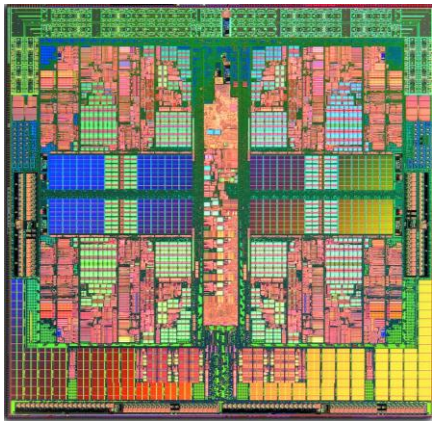
Beam forming for antenna arrays



Frequency synthesis and radio



Synchronisation of multicore chips



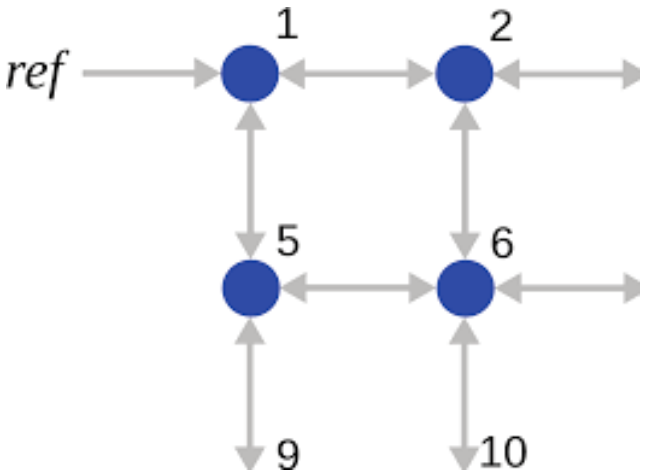
Pattern recognition and neuromorphic computing

ADPLL Network

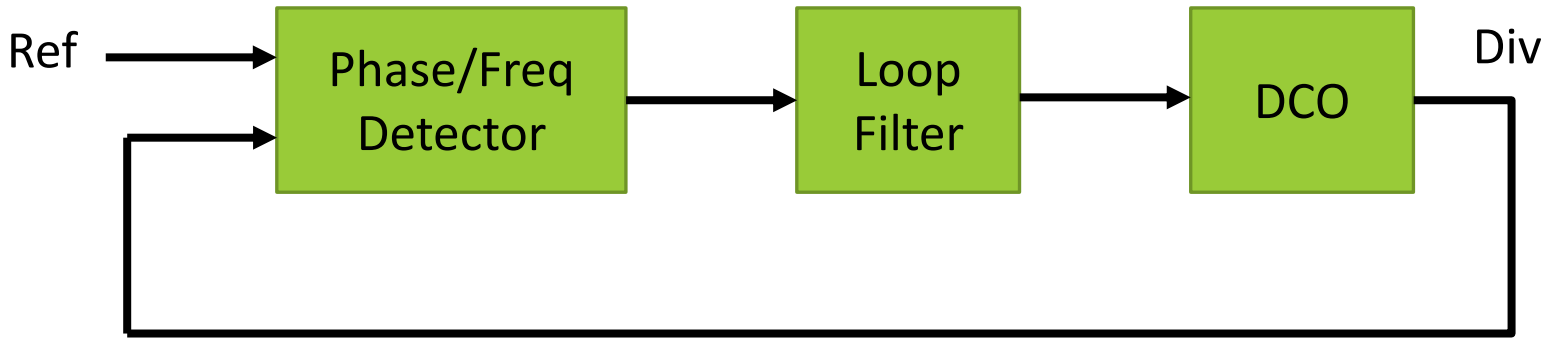
- Purpose: To spread a clocking signal in a large digital circuits with a minimal time delay and power consumption.

- Advantages:
  - Averaging of the jitter
  - Reduction of ADPLL noise

- Challenge:
  - Design low power & low jitter ADPLL
  - Small area ADPLL



ADPLL architecture



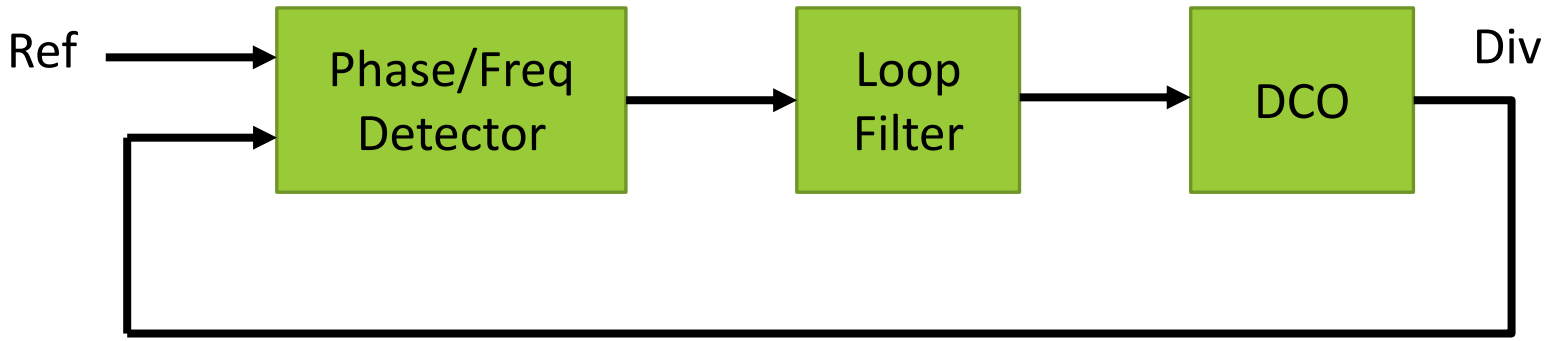
- **Basic blocks :**

  Phase-Frequency Detector (PFD) : determine a temporal error between the input Ref and the output Div

  Loop Filer: provide control signal

  DCO : digitally control oscillator

ADPLL architecture



- DCO comparison

LC oscillator	Ring inverter
Low Jitter	Low power consumption
Low phase noise	Small Area
	Low Frequency immunity to power supply variation

Proposed Work

- Design low jitter inverter ring DCO (few ps)

- DCO architecture suitable ADPLL network
  - Sub-mW DCO
  - Small area
  - good Frequency insensitivity to power supply variation

- Hybrid conversion scheme

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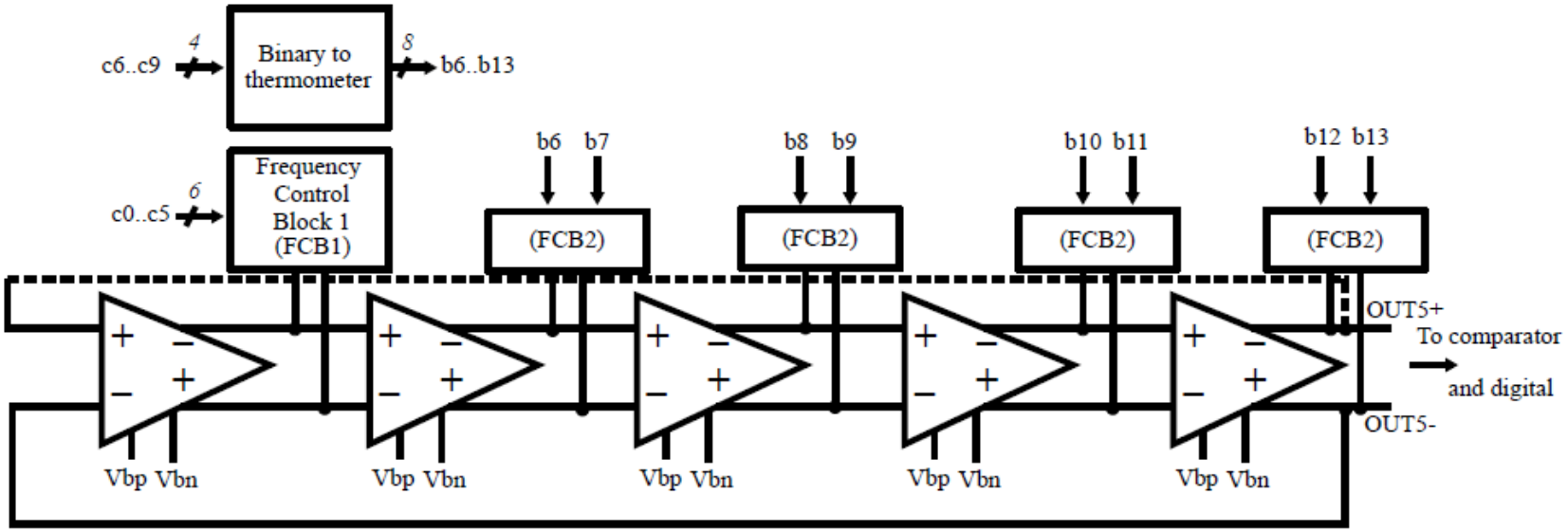
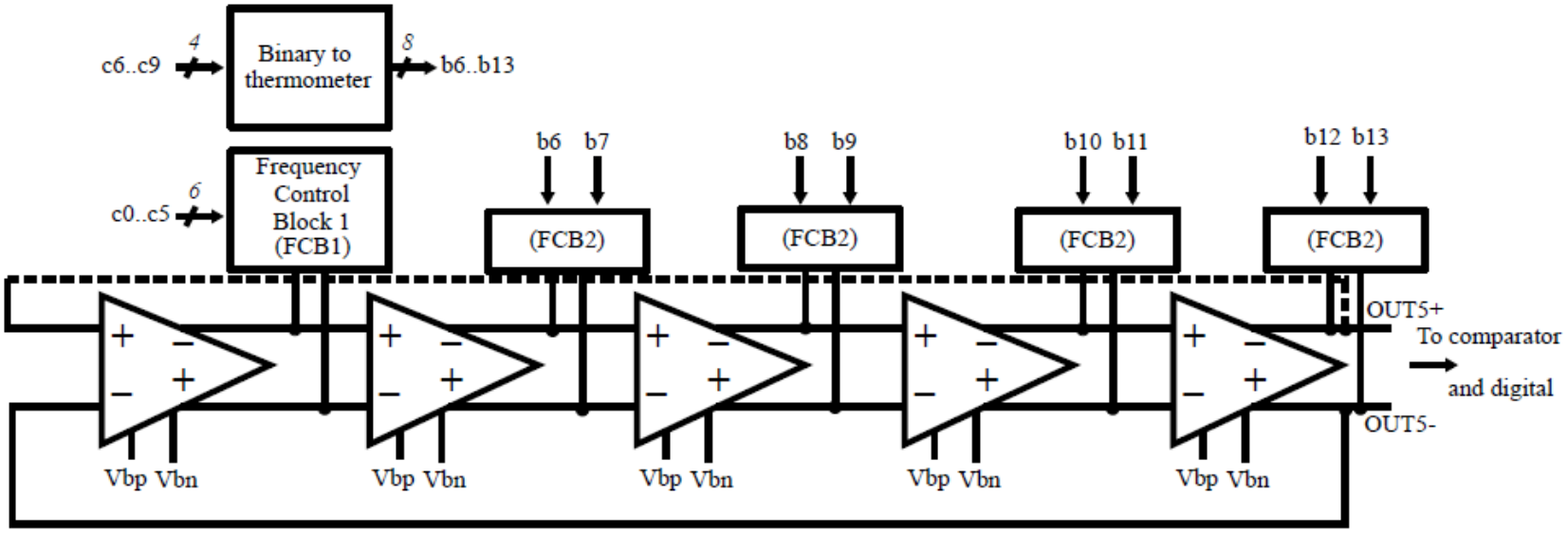
DCO Architecture

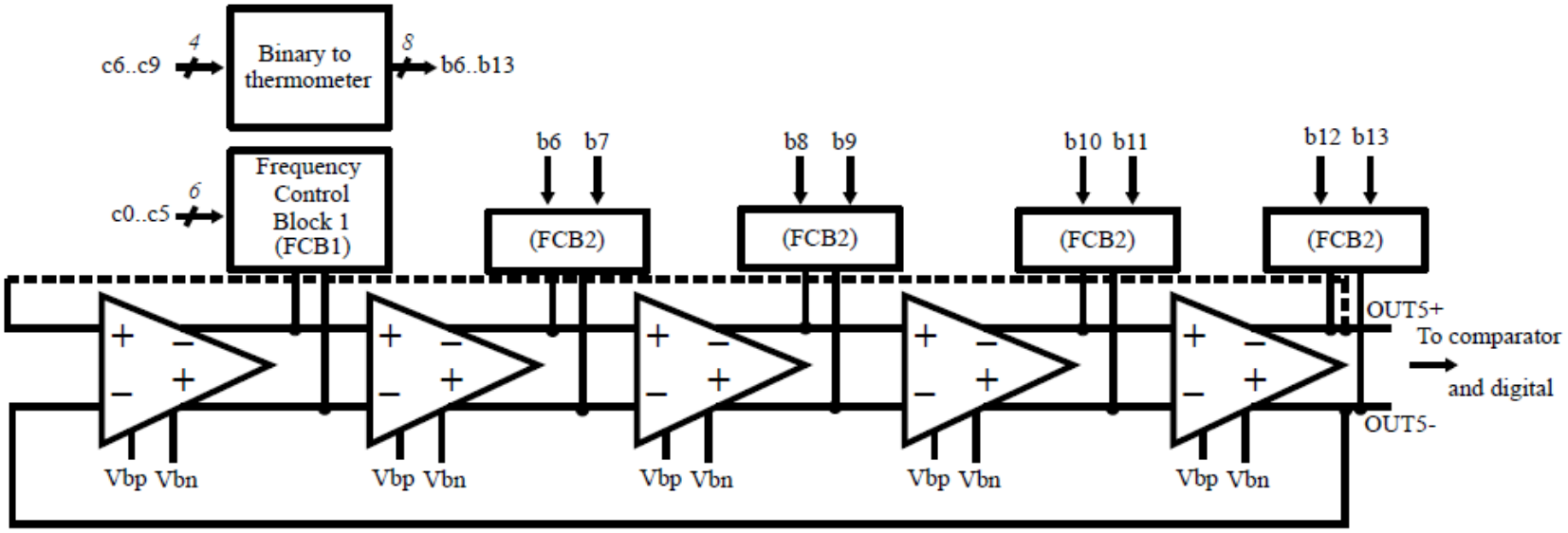


DCO Architecture



- 5 stages ring DCO
  - Good range of frequency
  - Split of C_L on all amplifier
  - Reduction of supply noise
- Binary to thermal conversion

DCO Architecture



- 5 stages ring DCO
  - Good range of frequency
  - Split of C_L on all amplifier
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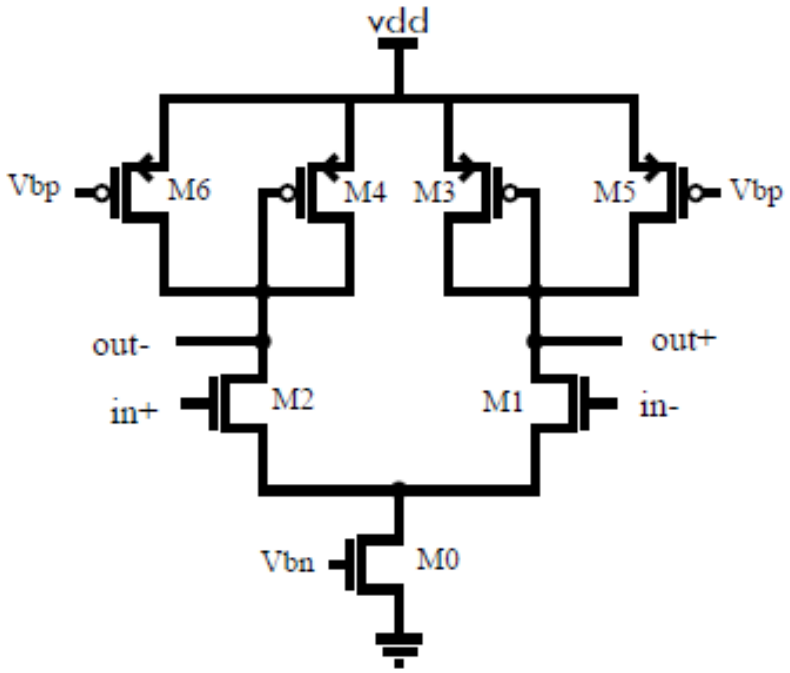
\+ immunity to power supply variation

\- Need for bias block & comparator

Differential Amplifier

- Constant current with M0 to avoid current peak
- Frequency defined by resistance load



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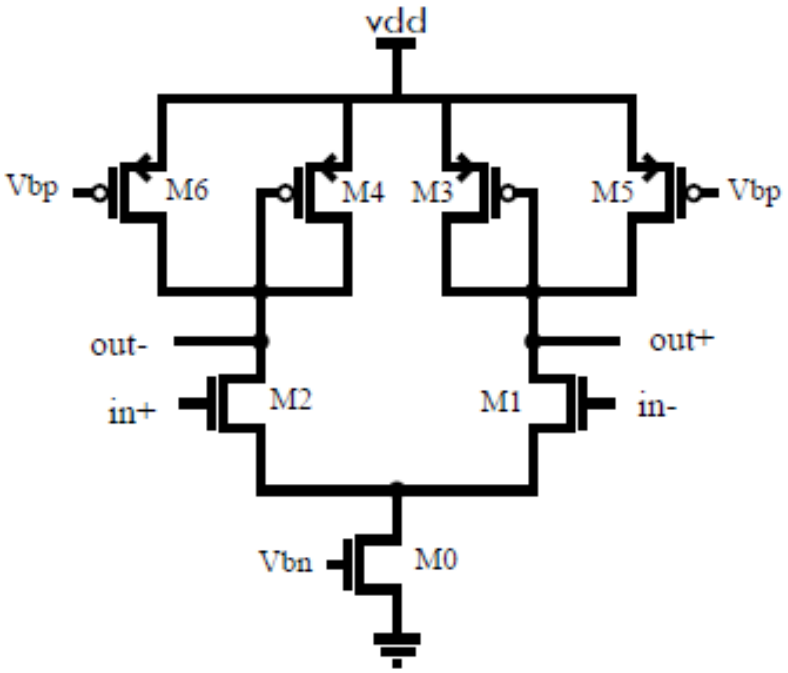
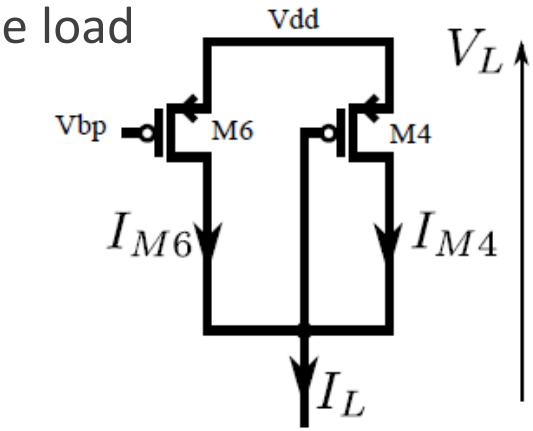
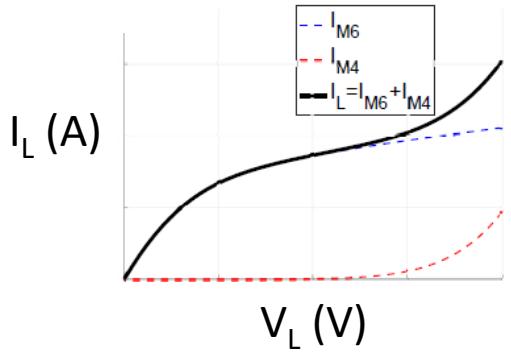
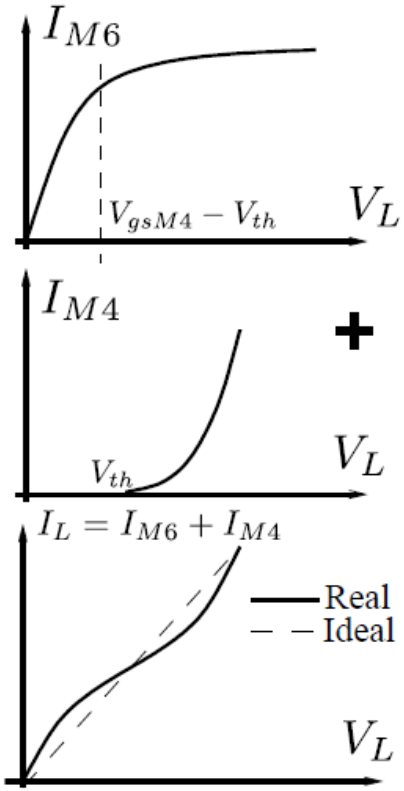
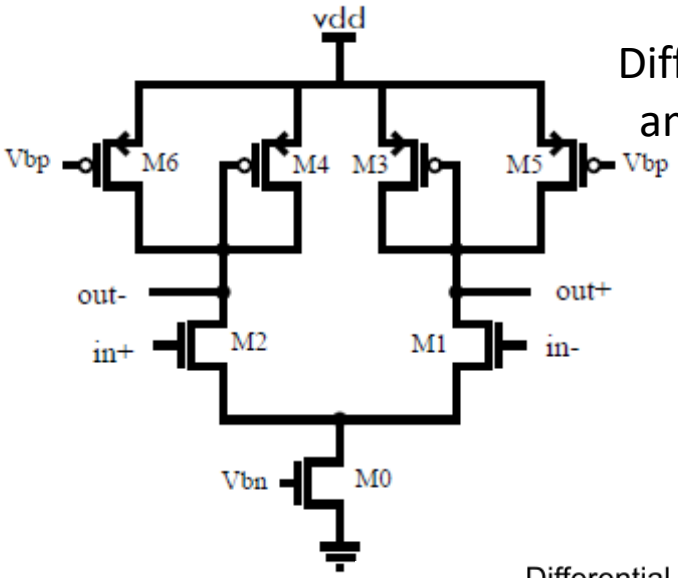








Transient response



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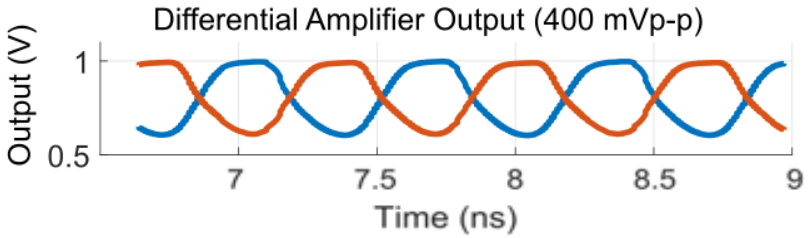

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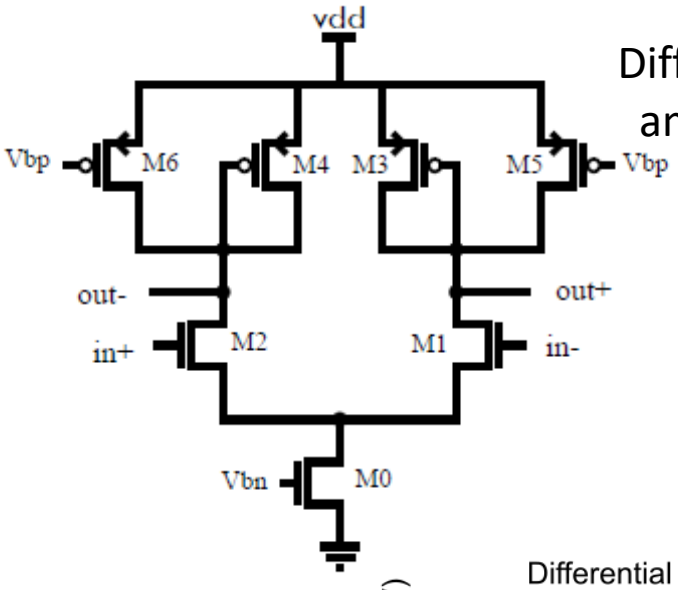

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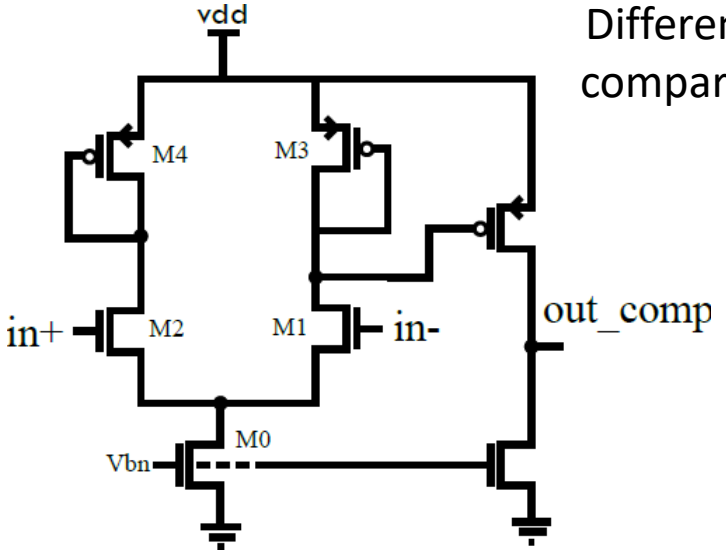
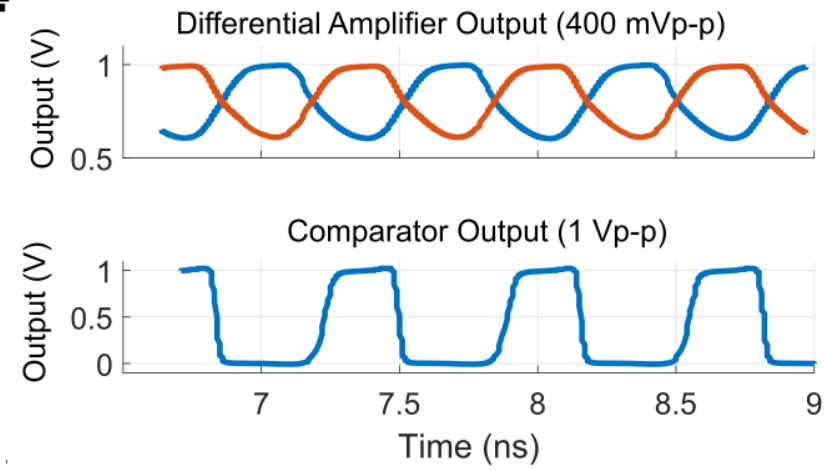
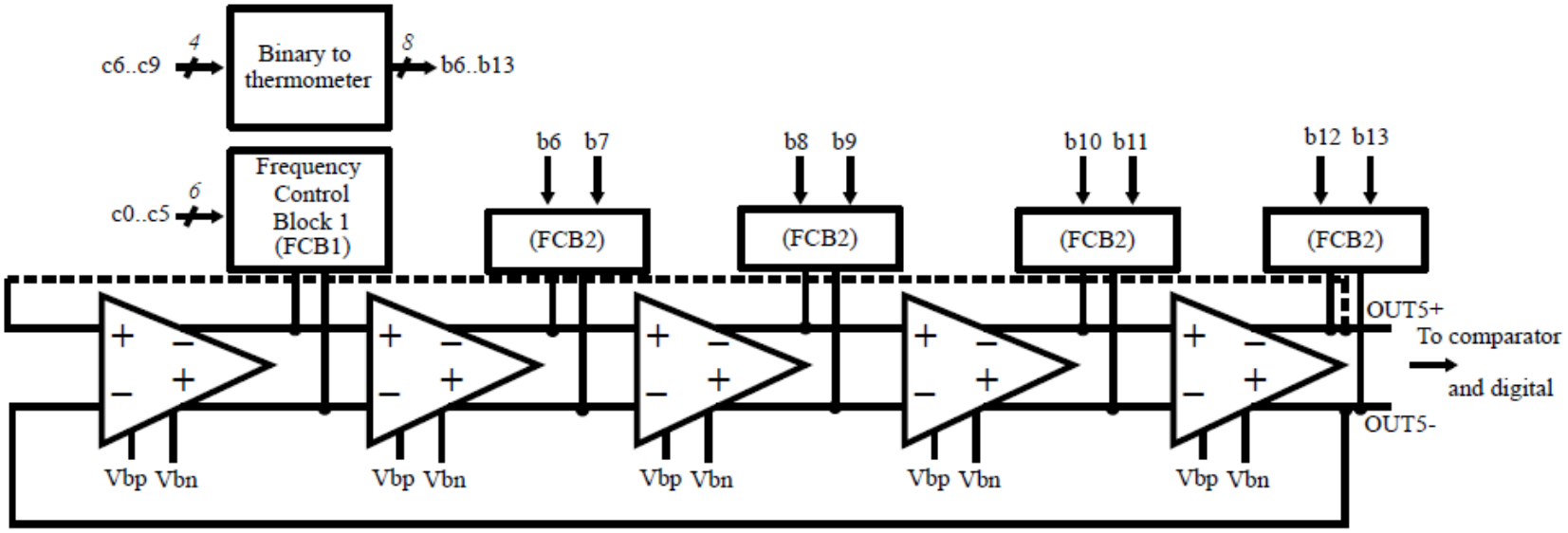


Differential comparator



Frequency Control (1)

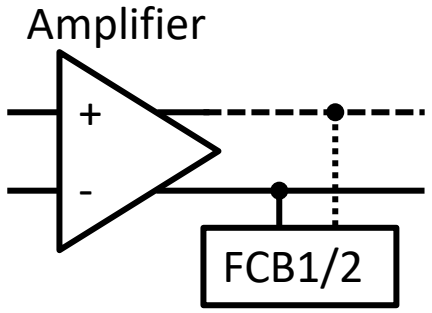


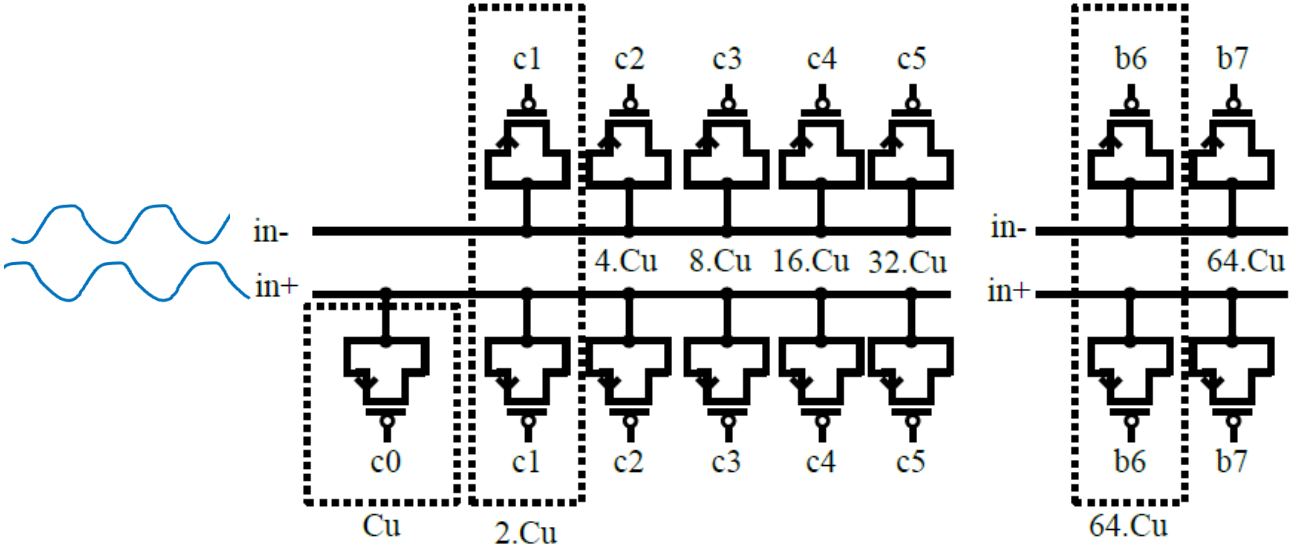
- Binary digital control : $c_{0..5}$
- Thermal digital control : $b_{6..13}$

Suitable control frequency : MOSCAP

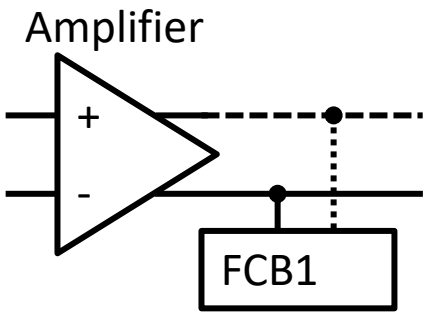
Frequency Control (2)

- FCB1 and FCB1 : bank capacitances using PMOS transistor
- PMOSCAP either in strong or weak inversion

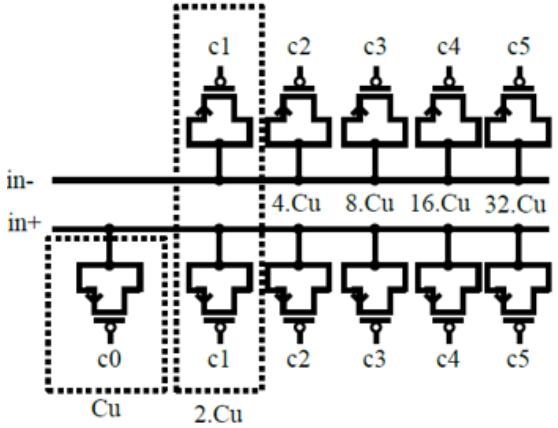




Frequency Control Layout Amplifier + FCB1



FCB1 block



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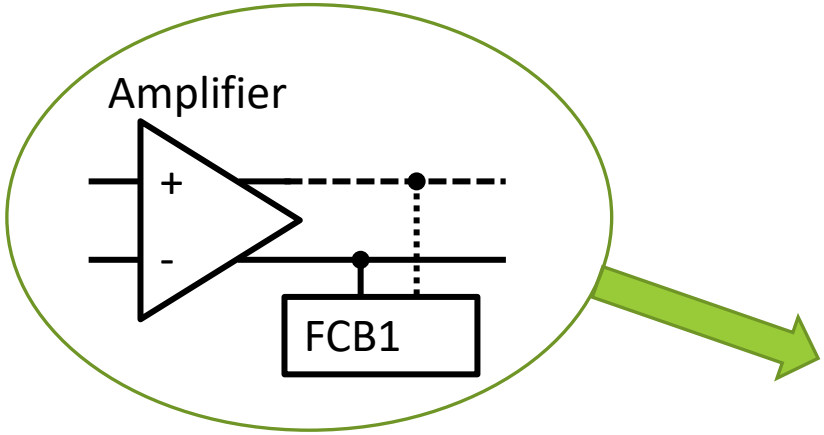
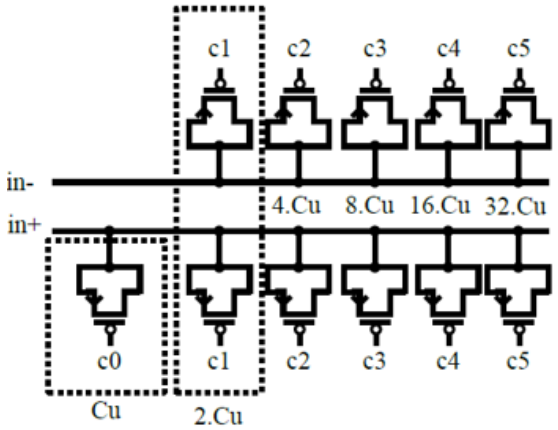
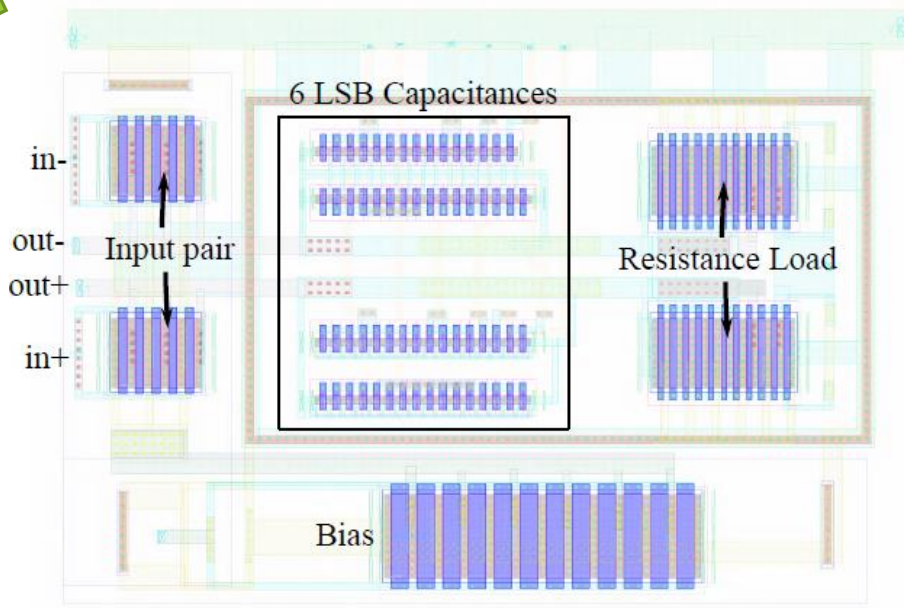


FCB1 block





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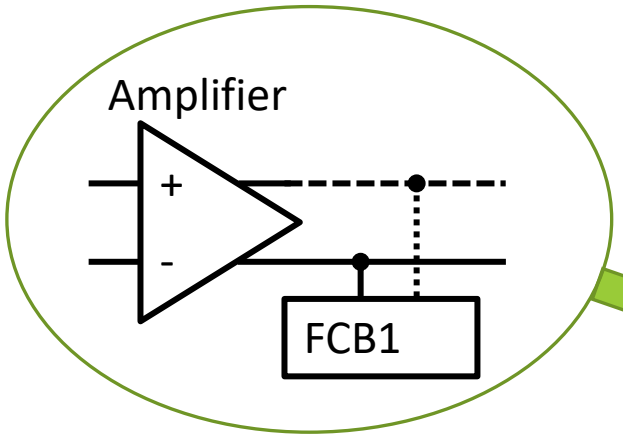

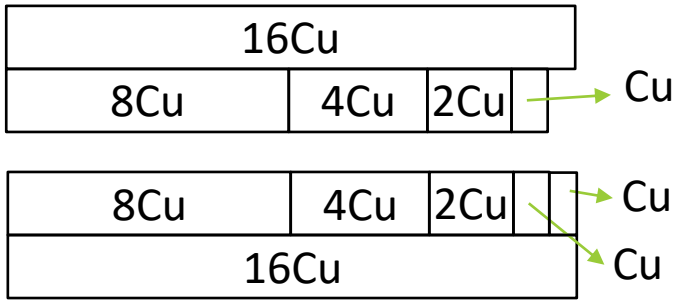

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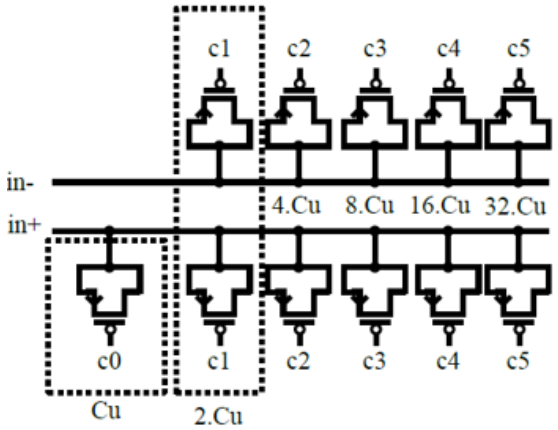
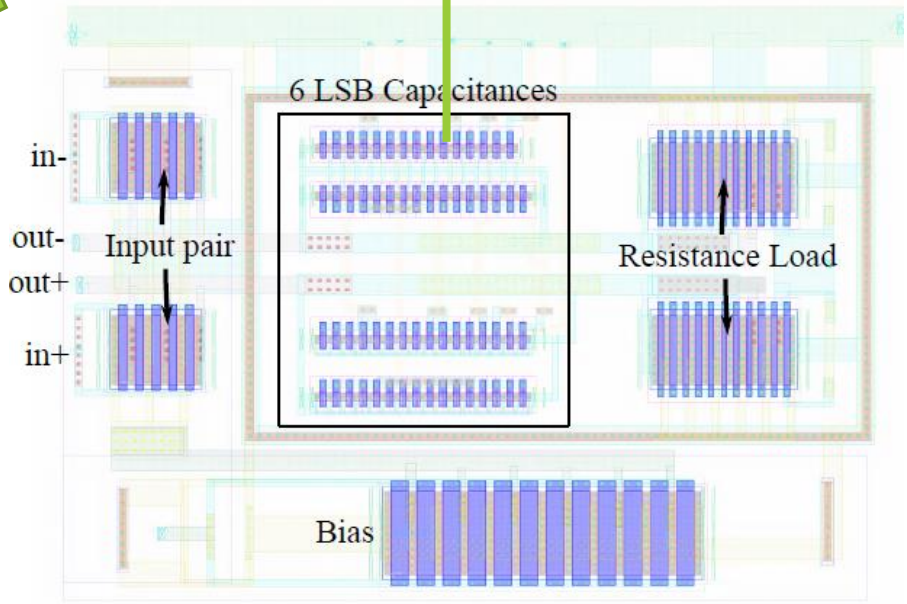
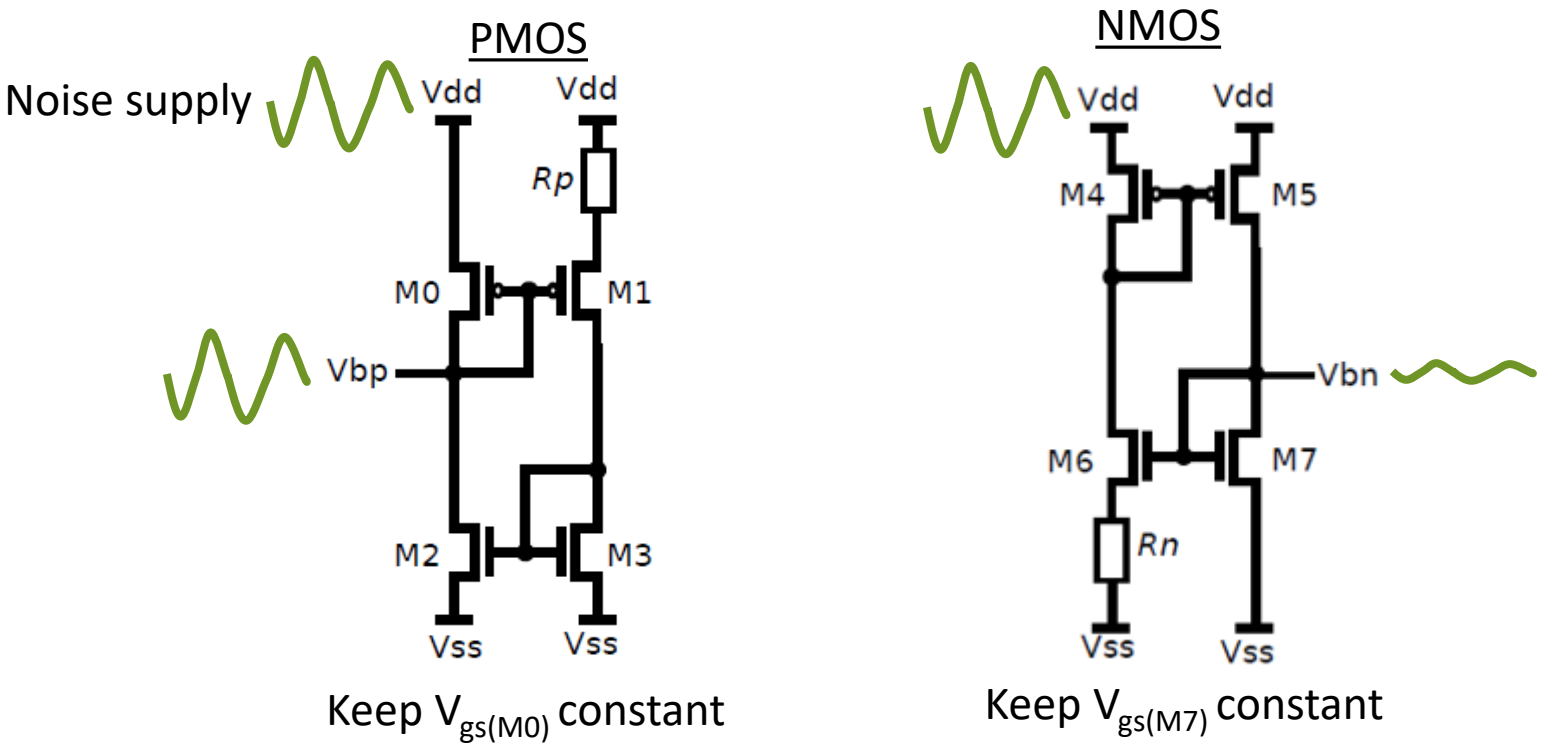




Bias Circuits

- PMOS and NMOS Bias voltage non sensitive to supply voltage variation



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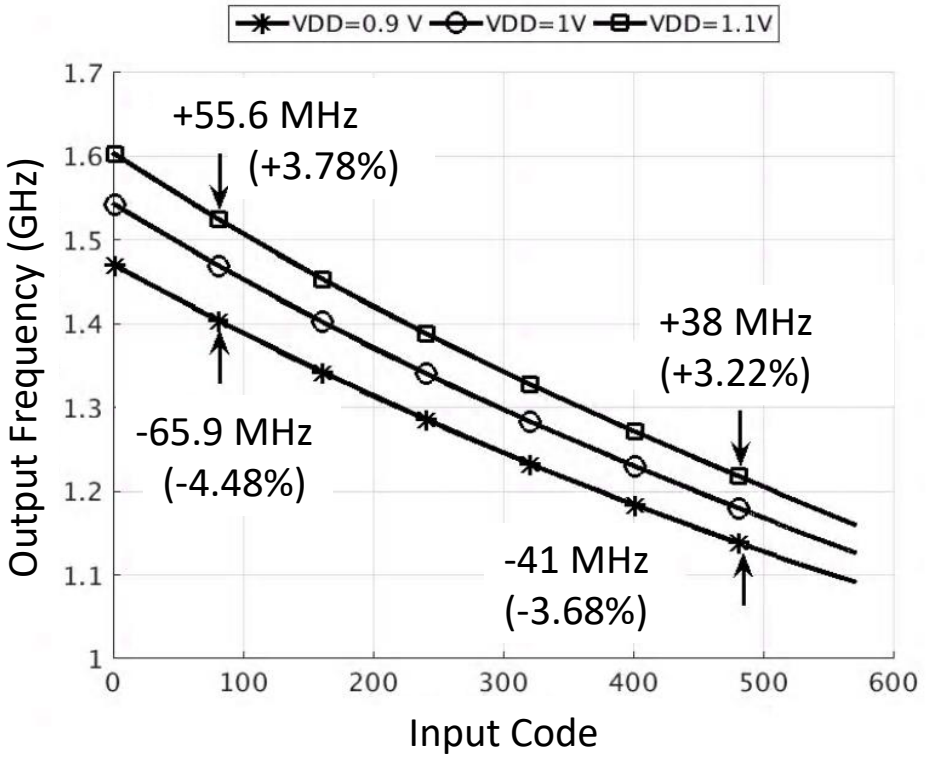
Frequency vs supply sensivity

- Single ended inverter ring : ± 20% frequency variation for ± 10% supply variation
- **Differential inverter ring** : ± 5% of frequency variation for ± 10% supply variation



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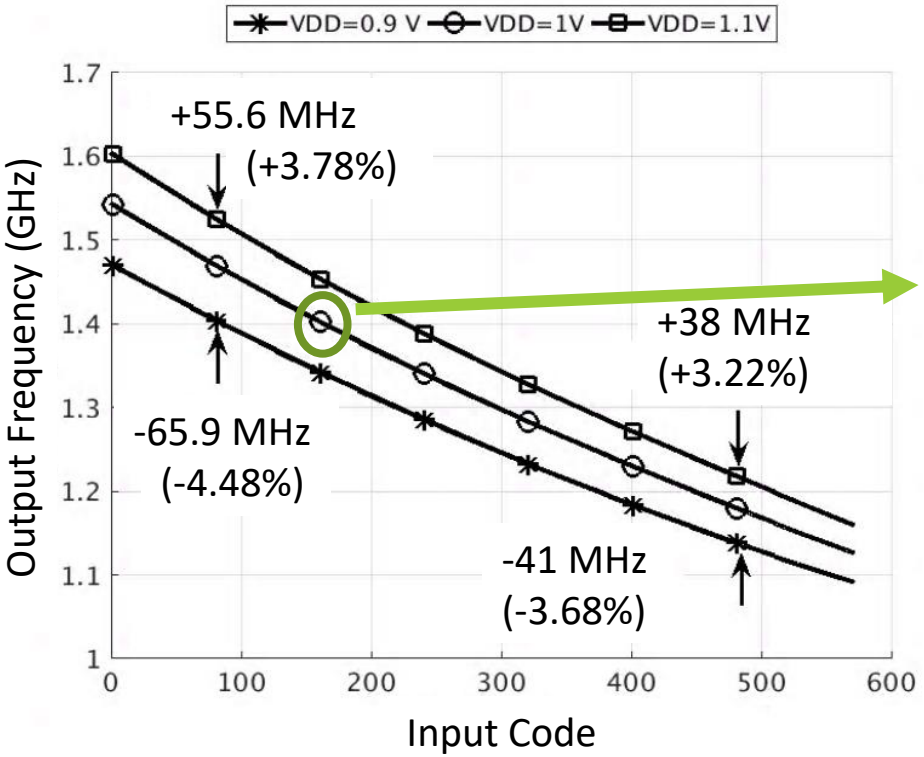
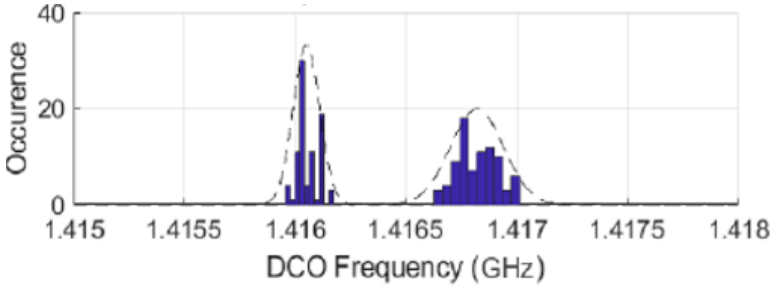
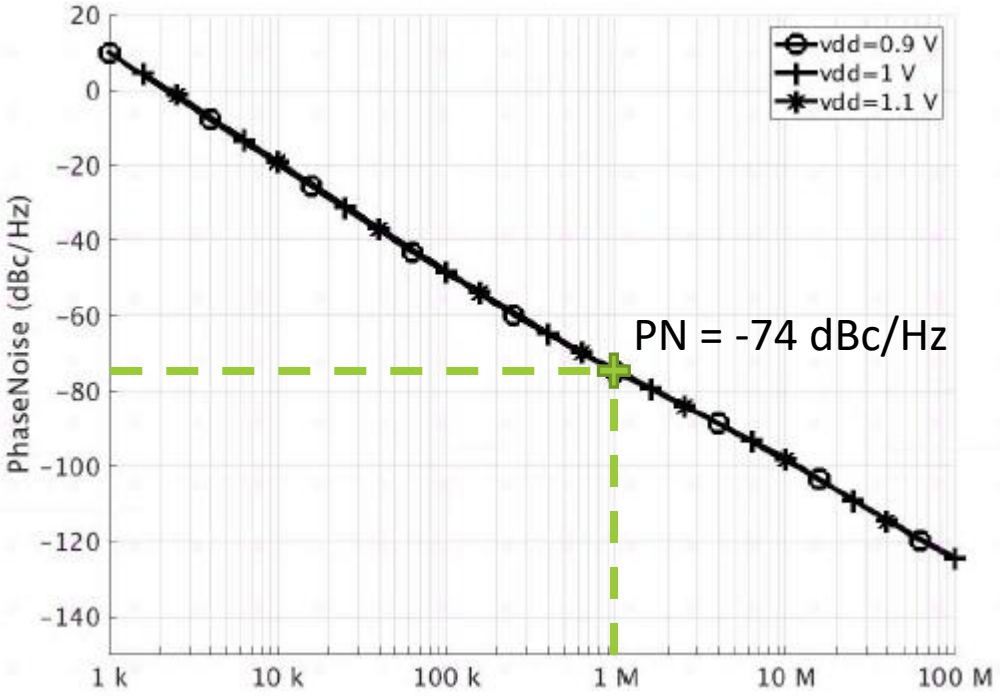


Transition between binary and thermal control



PSS Analysis

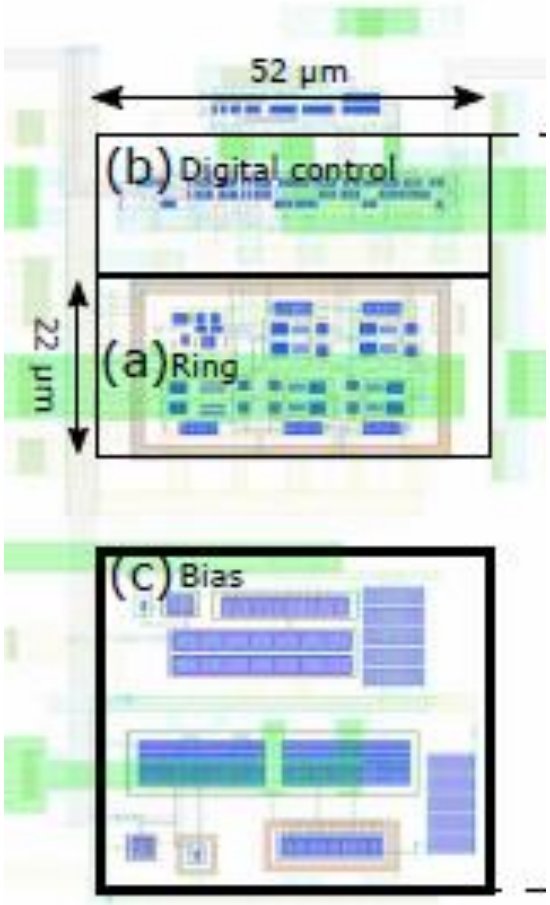
- Very good immunity to power supply variation
- Phase noise equivalent to a 2.3 ps jitter



DCO Performances and Layout

- Possibility to use one bias block for several DCO

Process	28 nm
Power Supply	1 V
Freq. Range	1.13 – 1.54 GHz
Control Code	576
Power Ring	660 µW
Power Digital control	102 µW @Fmax
Power Bias	81 µW



Comparison

- Good tradeoff for Area/power consumption/ frequency sensitivity to power supply

	[14]	[15]	[16]	This work
Tech(nm)	45	65	65	28
Supply(V)	1.1	1.2	0.85	1
Freq.(GHz)	0.547-10.49	1.5-3.5	0.9-1.4	1.13-1.54
Resolution(bit)	-	8	13	9
Power(mW)	0.783[3]	6	2.25	0.84
Area(μm^2)	170	156×92	90×210	108×52
PN (dBc/Hz)	-99.5[1] (@10MHz)	-	-96[2] (@1MHz)	-74[1] (@1MHz)
Jitter (ps)	-	1.6[1]	-	2.3[1]
FoM (dBc/Hz)	-145.9	-	-162	-135.5
FoM_T (dBc/Hz)	-207	-	-188	-163.2

[1] Post-layout simulation
[2] Chip measurement
[3] no DAC or frequency control implementation

Conclusion

- Design of differential DCO suitable for ADPLL network integration
- Hybrid binary/thermal control to optimize complexity and area
- Low jitter DCO and good immunity to voltage supply variation

Thank you for your attention