Design of Low-Temperature and Radiation-Hardened JFET Direct Coupled Op-Amps without Current Mirrors

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The purpose and novelty of the report is to develop the concept of the JFET direct coupled Op-Amps without current mirrors, which provides, first of all, the small values of the offset voltage's ($V_{\text{off}}$) systematic component.

In the report:

- the problem is posed and solved about the conditions for exclusion of the CMs in the JFET Op-Amp for the case when it is necessary to obtain a small $V_{\text{off}}$;
- shown that for this, three identical reference current sources should be used, which are implemented on the JFET transistors and the local negative feedback resistors;
- compares $V_{\text{off}}$ of the Op-Amp with the classic and proposed architecture;
- presents computer simulation results of the $V_{\text{off}}$ in the LTspice environment are presented, which show that silicon JFET direct coupled Op-Amps without CM have a systematic component of $V_{\text{off}}$ at the level of tens to hundreds of microvolts and voltage gain of more than 80 dB in a wide temperature range;
- the proposed solutions are relevant to successfully create JFET circuits for severe operating conditions, incl. based on Si JFET, SiC JFET, GaAs JFET.
### STRUCTURE OF THE REPORT

1. **CLASSICAL IMPLEMENTATION OF CURRENT MIRROR’S OP-AMPS**
2. **ZERO LEVEL OF TWO-STAGE OPERATING AMPLIFIER BASED ON CURRENT MIRROR**
3. **COMPONENT OF THE OFFSET VOLTAGE OP-AMP WITH CURRENT MIRRORS**
4. **INFLUENCE OF THE JFET CHANNEL LENGTH MODULATION EFFECT IN THE OP-AMP WITH CURRENT MIRRORS**
5. **THE ARCHITECTURE OF THE JFET OPERATIONAL AMPLIFIER WITHOUT CURRENT MIRRORS**
6. **COMPONENT OF THE OFFSET VOLTAGE OP-AMP WITHOUT CURRENT MIRRORS**
7. **THE PRACTICAL CIRCUIT OF THE JFET OPERATIONAL AMPLIFIER WITH SMALL $V_{\text{off}, N}$**
8. **COMPONENT OF THE OFFSET VOLTAGE AND GAIN OP-AMP WITHOUT CURRENT MIRRORS**
9. **THE JFET OP-AMP ON CASCODE COMPOSITE TRANSISTORS WITHOUT CURRENT MIRRORS**
10. **METHOD FOR INCREASING THE GAIN OF OP-AMPS WITHOUT CURRENT MIRRORS**
11. **CMRR OF THE OP-AMP WITH CURRENT MIRRORS**
12. **CMRR OF THE OP-AMP WITHOUT CURRENT MIRRORS**
13. **OP-AMP SIMULATION RESULTS WITHOUT CURRENT MIRRORS**
14. **EXAMPLES OF IMPLEMENTATION OF OP-AMP WITHOUT CURRENT MIRRORS**
15. **CONCLUSIONS**
Current mirrors are always based on bipolar transistors

Disadvantages:
- this circuit design does not contribute to ensuring a **low noise**;
- this circuit technique does not guarantee reliable operation of the op-amp when exposed to **cryogenic temperatures**;
- this circuit technique does not guarantee reliable operation of the op amp when exposed to **penetrating radiation**.
Fig. 1 To the Calculation of the Zero Level of the Two-Stage Op-Amp with Current Mirror CM1

In Fig. 1, the following designations are accepted:

- $I_{d1}, I_{d2}, I_{d3} = I_{R1}, I_{d4} = I_{R2}$ – drain currents of transistors M1, M2, M3 and M4;
- $V_{gs.3}, V_{gs.4}$ – gate-source voltages of transistors M3 and M4
ATTENTION! It should be noted that JFET current mirrors must contain field-effect transistors whose channel (p or n) is opposite to the type of channels of the Op-Amp input M1 and M2 transistors. This requirement further complicates the solution of the problem of constructing precision Op-Amps (due to the difference in the JFET drain-gate characteristics with n- and p-channels) on JFET current mirrors.
COMPONENT OF THE OFFSET VOLTAGE OP-AMP WITH CURRENT MIRRORS

If we take into account that the output current of CM1 and the drain current of transistor M2 are subtracted in the high-impedance node \(\Sigma_1\) (Fig. 1), then the offset voltage component due to the difference of \(K_i\) of the current mirror from unity can be found by the equation

\[
V_{\text{off}} = \frac{\Delta I_{\Sigma}}{g_{ds}}
\]

where \(\Delta I_{\Sigma} = 0.5 \cdot (I_{R1} + I_{R2}) \cdot (K_i - 1)\), \(g_{ds} \approx \frac{K_i + 1}{g_1^{-1} + g_2^{-1}}\) – slope of the conversion of \(v_{\text{in}}\) into the output current of the high-impedance mode \(\Sigma_1\); \(g_1, g_2\) – slope of the drain-gate characteristics of input transistors M1-M2.

In this way

\[
V_{\text{off}} \approx \frac{0.5 \cdot (K_i - 1) \cdot (I_{R1} + I_{R2}) \cdot (g_1^{-1} + g_2^{-1})}{K_i + 1}
\]

where \(I_{R1}, I_{R2}\) – currents in resistors R1, R2, the setting errors of which are determined by the variation of resistances (R1, R2), as well as the non-identity of the drain-gate characteristics of M3, M4.

Therefore, at \(K_i=1\) in the Op-Amp circuit of Fig. 1 the setting errors of currents \(I_{R1} (I_{R2})\) as well as their temperature and radiation dependences do not affect \(V_{\text{off}}\). This is the main advantage of the Op-Amp with the ideal current mirror.
INFLUENCE OF THE JFET CHANNEL LENGTH MODULATION EFFECT IN THE OP-AMP WITH CURRENT MIRRORS

However, in real CM circuits $K_i$ is affected not only by the technological spread of the input characteristics of the dominant transistors, but also by their Early voltage (for JFet this is the channel length modulation effect). As a result, to obtain $V_{\text{off}}=0$ in the Op-Amp Fig.1, the CM circuits are significantly complicated, which degrades the frequency properties of the Op-Amps and its dynamic parameters when processing the impulse signals. An alternative circuitry is necessary for the JFet Op-Amp.

A feature of the Op-Amp architecture with a current mirror Fig. 1 consists in the asymmetry (non-identity) of the static gate-drain voltages ($V_{gd}$) of the input transistors $M_1$ and $M_2$:

$$\Delta V_{gd.1-2} = V_{gd.1} - V_{gd.2} .$$

If in the diagram of Fig. 1 takes into account the effect of the JFet channel length modulation, which is characterized by an internal feedback coefficient for a common-gate circuit

$$\mu_i = \frac{\Delta V_{gs.i}}{\Delta V_{gd.i}} \bigg|_{I_s.i = \text{const}} = 10^{-2} \div 10^{-3} ,$$

it can be shown that an Op-Amp with a current mirror (Fig. 1) has an additional component of the offset voltage ($V^*_\text{off}$), which is present even with completely identical input $M_1$ and $M_2$ transistors: $V^*_{\text{off}} \approx \mu_0 \cdot \Delta V_{gd.1-2} ,$$

where $\mu_0 = \mu_1 = \mu_2$ are the numerical values of coefficient of the $M_1$ and $M_2$ transistors with their complete identity.
Thus, the asymmetry of the static mode of M1 and M2 transistors in the circuit Fig. 1 can become the dominant factor that has a significant effect on the parameters of an Op-Amp with a current mirror. Moreover, this effect is manifested even with ideal CM (when $K_i=1$) and significantly worsens not only $K_{CMRR}$, but also the common-mode rejection ratio (CMRR). To minimize this effect, it is necessary to use special CM [15], introduce a symmetrization circuit (equivalent voltage source $E_0$), which can ensure the equality, and rationally choose a constant component at the input of the BA. The use of cascode composite transistors instead of single M1 and M2 transistors also reduces the above-mentioned errors of the Op-Amp Fig. 1.
Fig. 2 Two-Stage JFET Op-Amp without Current Mirror with the High Identity of Three Sources of Reference Current $I_1 = I_2 = I_3$
COMPONENT OF THE OFFSET VOLTAGE OP-AMP WITHOUT CURRENT MIRRORS

If in the circuit of Fig. 2 the high identity of the sources of reference current $I_1=I_2=I_3$ is ensured in a wide range of supply voltages, temperatures and radiation effects, as well as the technological spread of the parameters of the elements, it can be shown that the architecture of the Op-Amp of Fig. 2 can, in a number of cases, compete with the classical application of the CMs in the Op-Amp, shown in Fig. 1. Indeed, the offset voltage of the Op-Amp of Fig. 2 ($V_{\text{off.N}}$) (if the static modes of M1 and M2 are identical in gate-drain voltage, which is provided by an auxiliary voltage source $E_0$), is determined by the equation

$$V_{\text{off.N}} = [I_3 - 0.5 \cdot (I_1 + I_2)] \cdot (g_1^{-1} + g_2^{-1})$$  \hspace{1cm} (3)

That is, in the circuit of Fig. 2, to get $V_{\text{off}}=0$, equality must be respected

$$I_3 = 0.5 \cdot (I_1 + I_2)$$  \hspace{1cm} (4)

In the BiJT and CMOS Op-Amps it is almost impossible to fulfill condition (4) with high accuracy. At the same time, the integrated JFETs make it possible to create the identical sources of reference current $I_3$, $I_2$, $I_1$, that is, to obtain small $V_{\text{off.N}}$. 

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Fig. 3 An Example of Constructing a Two-Stage JFET Op-Amp without Current Mirror
COMPONENT OF THE OFFSET VOLTAGE AND GAIN OP-AMP WITHOUT CURRENT MIRRORS

For the Op-Amp circuit of Fig. 3 with the architecture of Fig. 2 we can find that the offset voltage

\[ V_{\text{off.N}} = \left( g_1^{-1} + g_2^{-1} \right) \cdot \left[ I_R3 - 0.5 \cdot (I_{R1} + I_{R2}) \right] \]  \hspace{1cm} (5)

or

\[ V_{\text{off.N}} = \left( g_1^{-1} + g_2^{-1} \right) \cdot \left[ \frac{V_{gs5}}{R3} - \frac{V_{gs3}}{2R1} - \frac{V_{gs4}}{2R2} \right] \]  \hspace{1cm} (6)

In this case, the total gain of the Op-Amp is determined by the equation

\[ A_0 \approx A_2 \sqrt{\frac{\mu_2 + 2 \cdot \frac{\mu_5}{R3 \cdot g_0}}{}}. \]  \hspace{1cm} (7)

Thus, in the proposed JFET Op-Amp of Fig. 3 to obtain small \( V_{\text{off}} \approx 0 \) it is necessary to solve the problem of ensuring the identity of currents through resistors \( R1, R2 \) and \( R3 \), which are included in equation (7) as the ratio of quantities between which there is a correlation relationship (in the manufacture of the Op-Amps in a single technological process).
Fig. 4 The JFET Op-Amp with an Architecture of Fig. 3 on Cascode Composite Transistors
To reduce the dependences of currents $I_{R1}$, $I_{R2}$, $I_{R3}$ on the Op-Amp supply voltage, and to increase the open gain, it is advisable to use double (Fig. 4), and in some cases triple composite cascode structures as M3, M4, M5. Thus, the gain of the Op-Amp Fig. 4 takes values

$$A_0 \approx \frac{A_2}{\mu_2 \cdot \mu_2^* + 2 \frac{\mu_5 \cdot \mu_5^*}{R_3 g_0}}$$

where $\mu_2^*, \mu_5^*$ is the internal feedback coefficients of the transistors M2* and M5 * of the Op-Amp circuit of the Fig. 4.
For the Op-Amp with a current mirror of Fig. 1 (if transistors M1 and M2 are identical and operate with the same gate-drain voltages, and their internal feedback coefficients ($\mu$) in the common-gate circuit associated with modulation of the channel length JFet are close to zero), taking into account, we can find

$$\text{CMRR}_1 \approx \frac{2R_0}{g_1^{-1} + g_2^{-1}} \cdot (K_i - 1)$$

(9)

where $R_0 = R_{i3} || R_{i4}$ – equivalent output impedance of parallel reference current sources on transistors M3 and M4, besides

$$R_{i3} \approx R_3 \cdot \mu_3^{-1}, \quad R_{i4} \approx R_4 \cdot \mu_4^{-1},$$

$\mu_3 \approx \mu_4 = 10^{-2} \div 10^{-3}$ – internal feedback coefficient of M3, M4 in the common-gate circuit.
Thus, the presence of current mirror CM1 having $K_i = 1$ positively effects on CMRR of the Op-Amp of Fig. 1. However, it is difficult to implement the high-quality CMs on the JFET transistors and simple “cloning” of the well-known BJT and CMOS circuitry solutions does not provide to obtain $K_i$ close to unity. Moreover, in the known CM circuits, the relative difference of will reach $100 \div 200\%$. Therefore, the structure of the Op-Amp with current mirrors of Fig. 1 is promising only for the technological processes that ensure the construction of current mirrors on the bipolar and CMOS transistors. It should be noted that this solution does not allow for reducing the noise level of the Op-Amp, and also affects its performance in conditions of low temperatures and penetrating radiation.
Similarly, for the Op-Amp circuit without current mirrors (Fig. 2, Fig. 3), we can find that
\[
\text{CMRR}_2 \approx \frac{2R_0}{g_1^{-1} + g_2^{-1}}. \tag{10}
\]

The use of cascode switching of the transistors in the RCS (Fig. 4) provides the further increase in CMRR2 without current mirrors, since in this case
\[
R_{i3} \approx \frac{R \mu_3}{\mu_3^*}, \quad R_{i4} \approx \frac{R \mu_4^*}{\mu_4}. 
\]

Thus, the architecture of the Op-Amp (Fig. 2, Fig. 3, Fig. 4) allows us to obtain the acceptable values of CMRR.
OP-AMP SIMULATION RESULTS WITHOUT CURRENT MIRRORS

When modeling the Op-Amp, the authors of the paper used radiation-hardened and low-temperature models of silicon JFETs by Minsk JSC "Integral" (Belarus), which were verified on the basis of experimental studies at the Institute of Nuclear Problems of the Belarusian State University, and these transistors were built into the LTspice.

Graph Fig. 5 of the Op-Amp is obtained with the following element parameters:

- supply voltage is ± 5 V;
- M1 ÷ M5 transistors – "JN260_2" model, gate width = 260 μm, gate length = 2 μm;
- resistance of identical resistors $R_1=R_2=R_3=2 \, \text{kΩ}$.

The gain of the Op-Amp Fig. 4 at a $A_2=+1$ coefficient of the buffer amplifier and low temperatures (t=$-197^\circ \text{C}$) it has a value of 94.2 dB, and at room temperature (t=$27^\circ \text{C}$) it is 86.7 dB.

Fig. 5 Dependence of the Offset Voltage's Systematic Component of the Op-Amp Fig. 4 in the temperature range from -197 ° C to 30 ° C
EXAMPLES OF IMPLEMENTATION OF OP-AMP WITHOUT CURRENT MIRRORS

M1-M9 – JFET transistors;
CSE1, CSE2 – current stabilizing elements;
ES1 – special stabilizing element static mode;
BA – buffer amplifier;
$C_{corr}$ – corrective capacity
$E_{c1}$, $E_{c2}$ – auxiliary voltage sources;
$\Sigma_1$ is a high impedance node.
EXAMPLES OF IMPLEMENTATION OF OP-AMP WITHOUT CURRENT MIRRORS

M1-M9 – JFET transistors;
DS – differential stage;
BA – buffer amplifier;
$C_{\text{corr}}$ – corrective capacity
$E_{c1}, E_{c2}$ – auxiliary voltage sources;
$\Sigma_1$ is a high impedance node.

Fig. 7 CJFET High Voltage Gain Op Amp
CONCLUSIONS

1. A circuit technique has been developed that allows you to design a JFET direct coupled op-amp without current mirrors.

2. JFET direct coupled op-amp without current mirrors. The basic equations have been obtained for the offset voltage of the op-amp and the common-mode rejection ratio with the classical and proposed JFET architectures, which make possible to compare them. They show that the new CJFet Op-Amp circuitry could be an alternative to the JFET Op-Amp with current mirrors.

3. Computer simulations in the LTSpice environment showed that the systematic component of the silicon JFet Op-Amp's offset voltage without current mirrors does not exceed 150 µV in a wide temperature range and neutron flux up to $10^{12}$ n/cm$^2$ with a voltage gain of more than 80 dB;

4. The proposed op amps can be implemented on Si JFET, SiC JFET or GaAs JFET.
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